

**Remarks**

Claims 1-5, 7-18 and 20-25 are pending in the application.

**Claim rejections**

**Section 103**

Claims 1-5, 7-12 14-18 and 20-25 were rejected under 35 USC 103(a) as being unpatentable over Kadambi et al. (US 6,934,830) ("Kadambi") in view of Choquette (US 6,088,784). The Applicant respectfully traverses. The cited art cannot support the asserted rejection for at least the reason that it does not disclose a write-back mechanism or operation as recited in independent claims 1, 4, 15 and 23.

In the Response to Arguments portion of the Office Action, it is contended that Choquette's "global bypass unit has a write-back feature to the register file, which when in combination with Kadambi reads upon the claimed limitation." The Applicant respectfully disagrees. Choquette is completely silent with regard to a global bypass unit writing back to a register file. Indeed, this would be directly contrary to the purpose of a bypass circuit as described in Choquette, which is to "*reduce* the access rate to the register file ... " (Choquette, col. 1, lines 24-25) (emphasis added). "A bypass circuit ... allows data to *bypass* the register file ... so that the data can be used by an execution unit at the next clock cycle" (Choquette, col. 1, lines 34-36) (emphasis added). Thus, quite the opposite to what is contended in the Office Action, Choquette teaches *not* writing back to the register file.

Kadambi is also wholly devoid of any suggestion of writing back to the register file. In the discussion of claim 7, the Office Action argues that "[t]he combination of the global bypass and register pane functionality results in data being moved back based on a LRU scheme if the register pane is full of operands" (referring to Choquette's global bypass and Kadambi's register pane). Kadambi's FIG. 3, element 310 and col. 4, lines 40-49 are cited. However, Kadambi's functional block 310 is plainly labeled "Store Operands in Register Pane" – which describes writing to the register pane, not the register file. As for col. 4, lines 40-49, this passage reads as follows:

"Note that a number of different schemes can be used to determine which operands to overwrite. In one embodiment of the present invention, the new operands

are written over the least recently used (LRU) operands within register pane 102. This causes the most recently referenced operands to remain within register pane 102. In another embodiment, random operands are overwritten. In yet another embodiment, a round-robin scheme is used to determine which operands to overwrite. Note that this round-robin scheme has the advantage of being very fast."

Again, what is being described is not writing from the register pane to the register file, but writing from the register file to the register pane. Thus, neither Kadambi nor Choquette suggests a writeback mechanism as recited in the independent claims. Withdrawal of the rejection is therefore respectfully requested.

Claim 13 was rejected under 35 USC 103(a) as being unpatentable over Kadambi in view of Choquette, and further in view of Zaitzeva et al. (US 5,781,924) ("Zaitzeva"). The Applicant respectfully traverses. Claim 13 depends on claim 4 and is therefore allowable over Kadambi and Choquette for at least the reasons discussed above. Zaitzeva does not cure the deficiencies in Kadambi and Choquette and consequently claim 13 is further allowable over the combination of Kadambi, Choquette and Zaitzeva. Withdrawal of the asserted rejection is therefore respectfully requested.

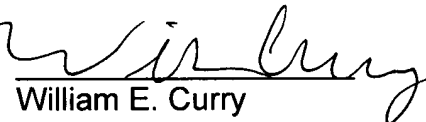
Conclusion

In light of the above discussion, Applicant respectfully submits that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Examiner is invited to contact the undersigned at (202) 220-4323 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

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